IEICE TRANS. ELECTRON., VOL.E91–C, NO.7 JULY 2008

INVITED PAPER *Special Section on Heterostructure Microelectronics with TWHM 2007*

Sb-Based n- and p-Channel Heterostructure FETs for High-Speed, Low-Power Applications

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SUMMARY Heterostructure field-effect transistors (HFETs) composed of antimonide-based compound semiconductor (ABCS) materials have intrinsic performance advantages due to the attractive electron and hole transport properties, narrow bandgaps, low ohmic contact resistances, and unique band-lineup design flexibility within this material system. These advantages can be particularly exploited in applications where high-speed operation and low-power consumption are essential. In this paper, we report on recent advances in the design, material growth, device characteristics, oxidation stability, and MMIC performance of Sb-based HEMTs with an InAlSb upper barrier layer. The high electron mobility transistors (HEMTs) exhibit a transconductance of 1.3 S/mm at V_{DS} = 0.2 V and an $f_T L_g$ product of 33 GHz-μm for a 0.2 μm gate length. The design, fabrication and improved performance of InAlSb/InGaSb p-channel HFETs are also presented. The HFETs exhibit a mobility of 1500 cm^2/V-sec, an $f_{\max}$ of 34 GHz for a 0.2 μm gate length, a threshold voltage of 90 mV, and a subthreshold slope of 106 mV/dec at V_{DS} = −1.0 V.

key words: *HEMTs, HFETs, MMICs, InAs, InGaSb*

1. Introduction

There is an expanding need to reduce power consumption in high-speed analog, digital, and mixed-signal circuits for military and commercial applications. Sb-based heterostructure devices have intrinsic high-speed and low-power consumption advantages that can provide the enabling technology needed for these applications, which include space-based communications, imaging, sensing, identification, high-data-rate transmission, micro-air-vehicles, wireless and other portable systems.

The low dc power consumption of AlSb/InAs HEMTs is attractive for large-scale active-array space-based radar applications which are particularly power-constrained. An f_T value of 110 GHz has been measured at V_{DS} = 100 mV and circuit demonstrations at L-, S-, X-, Ka-, and W-band have exhibited record low power dissipation [1]–[4]. Displacement damage radiation measurements show that they are also the most radiation tolerant HEMTs tested to date [5].

Recently, there has been considerable interest in the potential of III-V FET materials for advanced logic applications [6], [7]. A III-V high-speed, low-power complementary logic technology could enhance digital circuit functionality and sustain Moore's law for additional generations. When utilized in mixed signal circuits, a significant reduction in power consumption could also be obtained. For these applications, complementary circuits in the Sb-based material system would be highly desirable due to their low-power, high-speed advantages. To this end, p-channel HFETs having high hole mobility would be required.

In order to enhance the performance and reliability of Sb-based HEMTs and p-channel HFETs, the use of InAlSb as the upper barrier layer material has been investigated. When combined with an AlGaSb buffer layer, this design eliminates the use of the highly reactive AlSb material within the structure and simplifies the growth of an n^+ or p^+ cap layer above the InAlSb layer to enable lower access resistance [8]. In Sects. 2 and 3, we report on recent advancements at our laboratories on Sb-based HEMT material growth, fabrication, device characteristics, and MMIC performance utilizing this approach. In Sect. 4, recent developments on p-channel InAlSb/InGaSb HFETs at the Naval Research Laboratory are presented.

2. InAlSb/InAs HEMTs

The HEMT material was grown by solid-source molecular beam epitaxy (MBE) on a semi-insulating (100) GaAs substrate. Details of the growth procedures have been published elsewhere [9], [10]. A cross section of the material layer design is shown in Fig. 1. A 1.5 μm thick undoped $Al_{0.7}Ga_{0.3}Sb$ buffer layer is used to accommodate the 7% lattice mismatch. The upper barrier is 130 Å of $In_{0.2}Al_{0.8}Sb$. A GaTe source is used for Te delta-doping 65 Å above the channel. The electron sheet carrier density and mobility of the starting material at 300 K were measured to be 0.9×10^{12} cm^{-2} and 19,000 cm^2/V-s, respectively.

X-ray diffraction measurements demonstrate that the channel and upper barrier layers are nearly coherent with respect to the relaxed AlGaSb buffer layer, with the InAs in tension (1.1% mismatch) and the InAlSb in compression (1.3% mismatch). The electron density in the channel was controlled by varying the Te dose, with room-temperature mobilities between 18,000 and 25,000 cm^2/V-s for densities between 0.9×10^{12} and 2.4×10^{12}/cm^2.

The HEMTs were fabricated using evaporated Pd/Pt/Au source and drain ohmic contacts which were defined using PMMA resist and deep-UV lithography. The contacts were heat treated using a hot-plate. The gate was then

Manuscript received January 31, 2008.

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DOI: 10.1093/ietele/e91–c.7.1050

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
JAN 2008		**00-00-2008 to 00-00-2008**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Sb-Based n- and p-Channel Heterostructure FETs for High-Speed, Low-Power Applications	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Naval Research Laboratory,4555 Overlook Avenue SW,Washington,DC,20375**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT **unclassified**	b. ABSTRACT **unclassified**	c. THIS PAGE **unclassified**	**Same as Report (SAR)**	**8**	

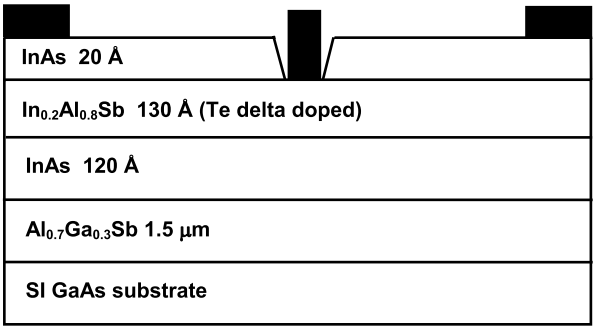

Fig. 1 InAlSb/InAs HEMT layer design.

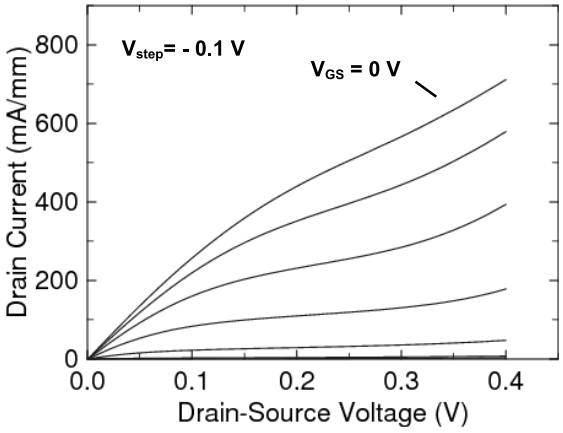

Fig. 2 InAlSb/InAs HEMT drain characteristics. $L_G = 0.2\,\mu$m, $L_{DS} = 0.6\,\mu$m, $W_G = 28\,\mu$m, $V_{GS} = -0.1$ V/step.

formed using PMMA e-beam lithography and lift-off techniques. Prior to deposition, the sample was given an O_2 plasma etch, followed by a 15 s etch in a citric-acid-based solution to remove the InAs cap layer. Finally, device isolation was achieved by wet chemical etching. With this etch, a gate air bridge was formed which extends from the channel to the gate bonding pad.

The drain characteristics obtained for a HEMT with a $0.2\,\mu$m gate length are shown in Fig. 2. The on-resistance at $V_{DS} = 50$ mV is $0.34\,\Omega$-mm for the $0.6\,\mu$m source-drain spacing. The maximum transconductance at $V_{DS} = 0.2$ V and 0.3 V is 1.3 S/mm and 1.7 mS/mm, respectively, as shown in Fig. 3. The values are comparable to the highest reported in any FET technology at these drain voltages. From the TLM measurements shown in Fig. 4, the ohmic contact resistance is estimated to be $0.03\,\Omega$-mm. The S-parameters of the HEMTs were measured on-wafer from 1 to 40 GHz. Based on the usual 6 dB/octave extrapolation, an f_T of 135 GHz and an $f_{\max}$ of 110 GHz were obtained at $V_{DS} = 0.35$ V and $V_{GS} = -0.25$ V. After removal of the gate bonding pad capacitance from an equivalent circuit, an intrinsic f_T of 165 GHz was obtained. This value corresponds to an $f_T L_g$ product of 33 GHz-μm.

AlSb is well known to oxidize rapidly when exposed to air. The oxidation stability of the InAlSb/InAs HEMTs was investigated to determine the reactivity of the InAlSb

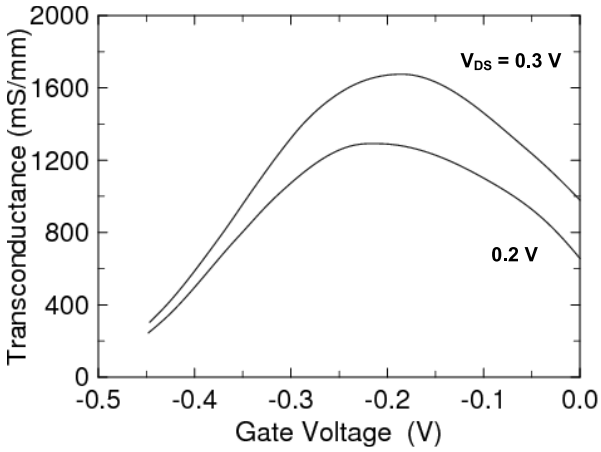

Fig. 3 HEMT transconductance vs. gate voltage.

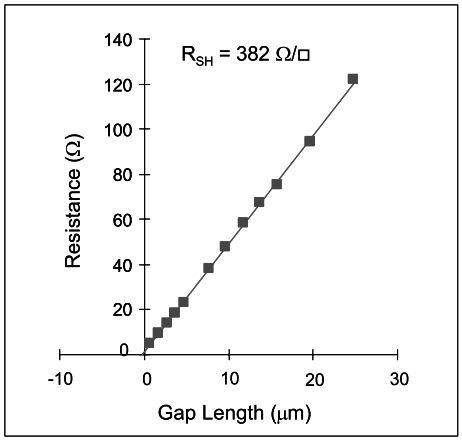

Fig. 4 TLM measurement on InAlSb/InAs HEMT material.

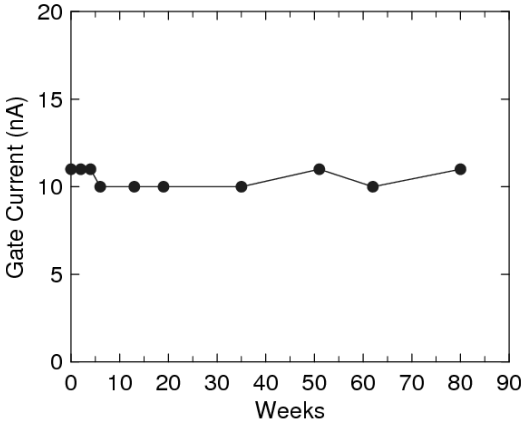

Fig. 5 Gate current stability measurements vs. time.

barrier layer. In this study, the gate current at $V_{DS} = 50$ mV and $V_{GS} = 0$ V on unpassivated HEMTs was monitored as a function of time in air. As shown in Fig. 5, the variation in the gate current after 80 weeks was only 1 nA, indicating the marked improvement in stability when In is added to the AlSb barrier material. Similar measurements of the

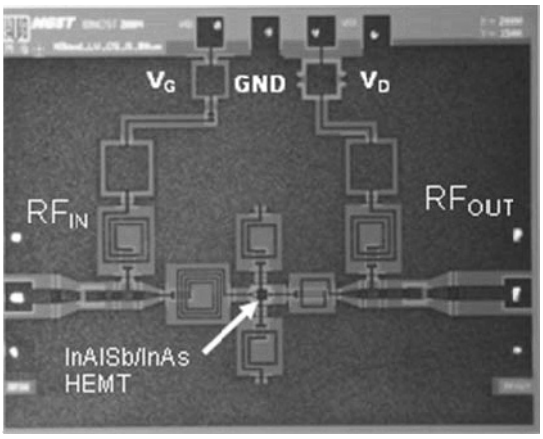

Fig. 6 Photograph of an InAlSb-InAs HEMT LNA.

drain current and gate current near pinch-off also revealed no significant change after 80 weeks.

The first InAlSb/InAs HEMT MMICs have also been recently demonstrated [11]. A photograph of the MMIC is shown in Fig. 6. The 0.1 μm gate-length HEMTs in these MMICs exhibit an f_T of approximately 220 GHz when biased at V_{DS} = 0.3 V and V_{GS} = −0.3 V. This value is comparable to those obtained previously for HEMTs with an InAlAs/AlSb barrier. With only 2 mW power dissipation, the X-band MMICs exhibited an associated gain and noise-figure at 12 GHz of approximately 12 dB and 3 dB, respectively, and an rf yield greater than 80%.

3. InAlSb/InAs HEMTs with an n^+ Cap Layer

The use of n^+ cap layer structures to enable non-alloyed, low resistance ohmic contacts and a reduction in the source-drain access resistance has been effectively utilized in InP-based HEMTs [12]. The use of an n^+ cap layer has also been demonstrated in Sb-based HEMTs with an InAlAs/AlSb upper barrier layer [13]. For Sb-based HEMTs, the InAlAs layer typically employed in the top barrier is in tensile strain with a 5.5% mismatch with the buffer layer [14]. Replacement of this layer with an InAlSb layer which is compressively-strained with a mismatch of only 1.3% would facilitate advanced cap layer designs in Sb-based HEMTs. The benefits of such a replacement are improved quality and reproducibility of the cap and barrier layer material, improved cap layer design flexibility, and a more controllable gate recess etch process, particularly when etching through a thin highly-doped barrier layer is required. In this section, we report on the material growth and device characteristics of the InAlSb/InAs HEMTs with an n^+ cap layer.

A cross section of the material layer design is shown in Fig. 7. A Te delta-doped layer was inserted within the 90 Å InAlSb barrier layer, and was located 65 Å above the channel. The nominal carrier density of the 200 Å thick n^+ InAs(Te) cap layer is 1×10^{19} cm^{-3}. A wafer map of sheet resistance is shown in Fig. 8. The uniformity is good, with an average value of 79.3 Ω/□ and a standard deviation

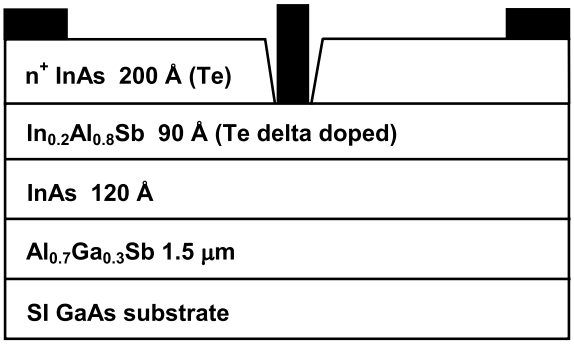

Fig. 7 InAlSb/InAs HEMT material with n^+ cap layer.

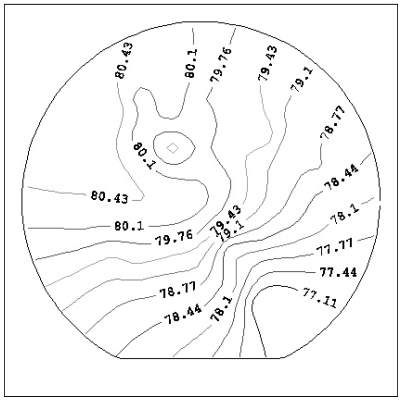

Fig. 8 Sheet resistance (Ω/□) uniformity of HEMT starting material with n^+ cap layer; wafer diameter is 76 mm.

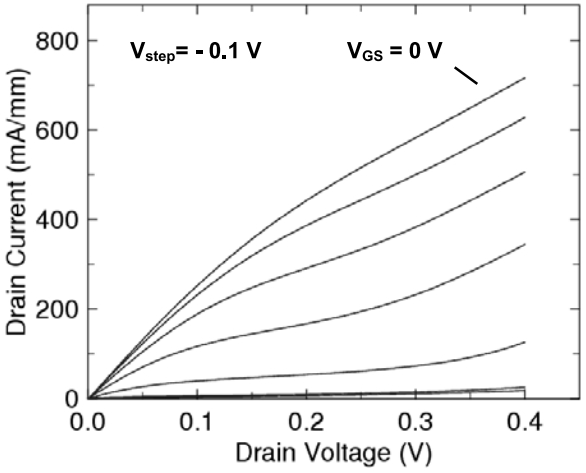

Fig. 9 Drain characteristics of InAlSb/InAs HEMT with n^+ cap layer. L_G = 0.28 μm, L_{DS} = 1.7 μm, W_G = 28 μm, V_{GS} = −0.1 V/step.

of 0.96 Ω/□. Hall measurements performed on the starting material indicated a sheet resistance of 89 Ω/□. Hall measurements were also performed on the starting material after removal of the n^+ cap layer using a selective chemical etch. The sheet carrier density and mobility at 300 K were 2.0×10^{12} cm^{-2} and 23,200 cm^2/V-s, respectively. The rms surface roughness after removal of the n^+ cap layer was 1.9 nm for a 5×5 μm^2 area. Atomic force microscopy mea-

surements were also performed on the heterostructure surface after a gate recess etch in the resist opening (bi-level PMMA/PMMA-MAA) prior to gate metal definition. In this case, the rms surface roughness after removal of the n^+ cap layer was 1.6 nm.

The HEMTs were fabricated as previously described except that a recess etch time of 120 seconds was employed to ensure etching through the thicker cap layer. The drain characteristics obtained for a HEMT with a 0.28 μm gate length are shown in Fig. 9. The on-resistance at 50 mV is 0.35 Ω-mm for the 1.7 μm source-drain spacing. The maximum transconductance at V_{DS} = 0.2 V and 0.3 V is 1.3 and 1.75 S/mm, respectively, as shown in Fig. 10. These values are comparable to those obtained in the previous section. From on-resistance measurements as a function of source-drain spacing of HEMTs fabricated on the same wafer, the ohmic contact resistance is estimated to be 0.03 Ω-mm as shown in Fig. 11 [13]. The sheet resistance obtained from this measurement is 126 $\Omega/\square$. To illustrate the effect of the n^+ cap layer, the values obtained for HEMTs with a 20 Å undoped cap layer and a 50 Å n^+ cap layer are also included in Fig. 11. For a 2 μm source-drain spacing, the HEMT on-resistance is reduced by more than a factor of 3. Further reduction in the source-drain resistance can be expected with the implementation of advanced n^+ cap layer designs.

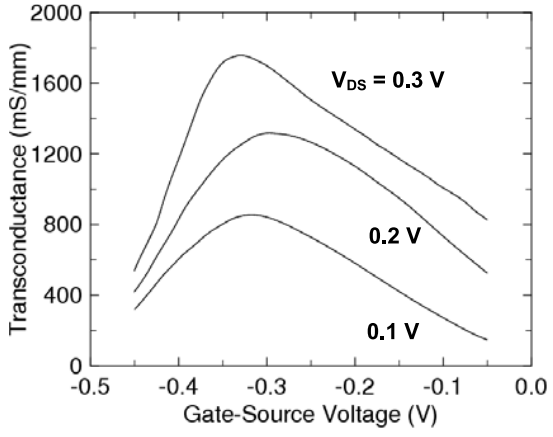

Fig. 10 Transconductance vs. gate voltage of InAlSb/InAs HEMT with n^+ layer.

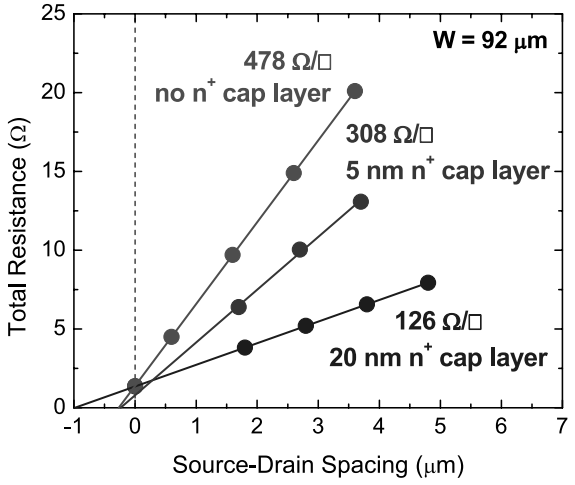

Fig. 11 HEMT on-resistance comparison on material with and without n^+ cap layers.

The S-parameters of the HEMTs were measured on-wafer from 1 to 40 GHz. Based on the usual 6 dB/octave extrapolation, an f_T of 80 GHz and an f_{max} of 90 GHz were obtained at V_{DS} = 0.3 V and V_{GS} = −0.4 V. After removal of the gate bonding pad capacitance from the equivalent circuit, an intrinsic f_T of 90 GHz was obtained, corresponding to an f_T-L_g product of 25 GHz-μm. HEMTs fabricated from this material with a 0.2 μm gate length exhibited an intrinsic f_T of 130 GHz and an f_{max} of 120 GHz. Higher f_T-L_g products can be expected with a shorter source-drain spacing. The f_{max} values obtained on the HEMTs with and without the n^+ cap layer should improve with the implementation of a low-gate-metal-resistance T-gate structure.

4. InAlSb/InGaSb p-Channel HFETs

For p-channel HFETs in complementary circuits, the $In_xGa_{1-x}Sb$ alloy system is attractive since the binary endpoints have the highest bulk hole mobilities of any III-V compound and a significant valence band barrier to enable quantum confinement [15]–[17]. This potential can be enhanced by using compressive strain to produce advantageous band splitting. As work in this direction, in this section we report on the fabrication and improved performance of Sb-based p-channel HFETs with an InAlSb/AlGaSb barrier, a strained, high-mobility, $In_{0.41}Ga_{0.59}Sb$ quantum well channel, and no highly-reactive AlSb material within the structure.

The Sb-based HFET material was grown by MBE on a semi-insulating (100) GaAs substrate. A 1.5 μm undoped $Al_{0.8}Ga_{0.2}Sb$ buffer layer was used to accommodate the 7% lattice mismatch. A cross section of the material layer design is shown in Fig. 12. Details of the growth procedures have been reported elsewhere [18]. The $In_{0.41}Ga_{0.59}Sb$

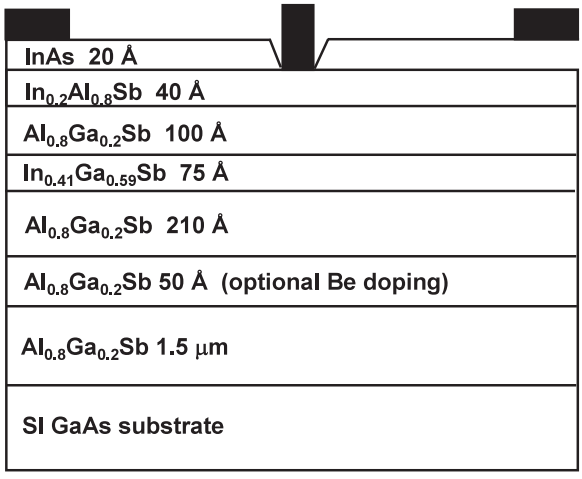

Fig. 12 InAlSb/InGaSb p-channel HFET layer design.

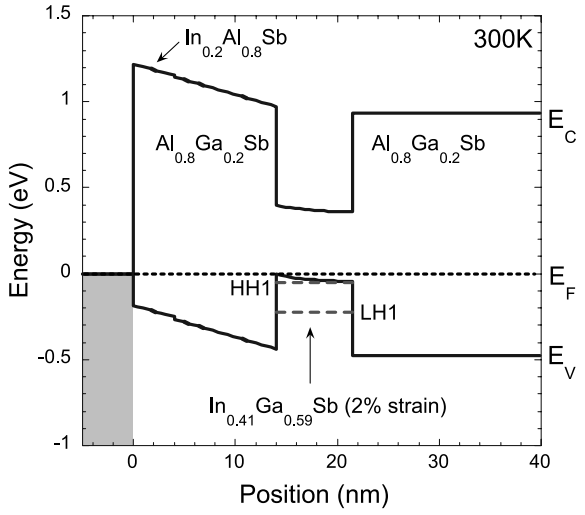

Fig. 13 p-Channel HFET energy-band diagram.

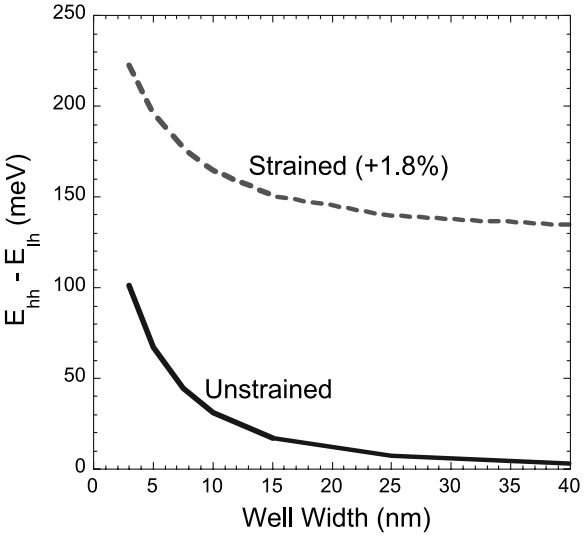

Fig. 14 Heavy hole and light hole energy separation dependence on well width for strained and unstrained conditions.

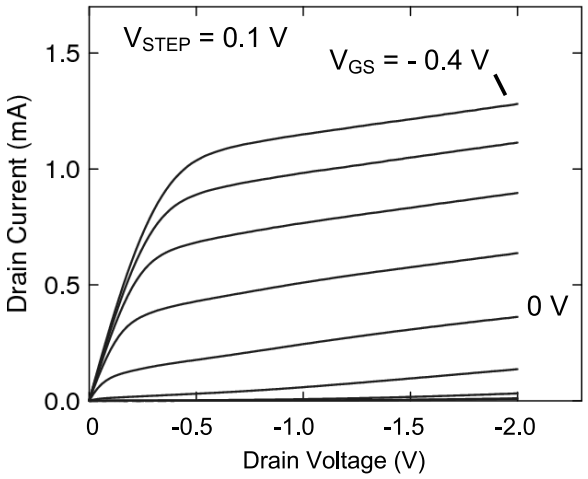

Fig. 15 HFET drain characteristics. $L_G = 0.25\,\mu$m, $L_{DS} = 1.0\,\mu$m, $W_G = 28\,\mu$m, $V_{GS} = 0.1$ V/step.

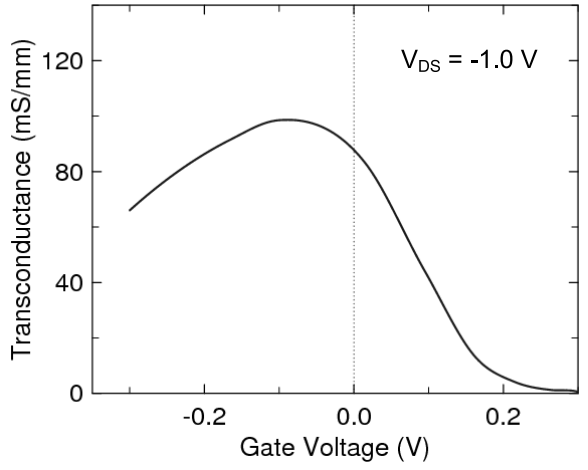

Fig. 16 p-Channel HFET transconductance vs. gate voltage.

channel layer is in a state of biaxial compressive strain since it was grown epitaxially on the relaxed AlGaSb buffer layer. The strain is about 2% for this particular composition. Modulation doping below the channel has previously been achieved using a 5 nm Be-doped AlGaSb layer. This optional doping scheme can enhance the capability for future scaling to ultra-thin gate-channel separations. A band diagram of the structure is shown in Fig. 13.

The band diagram and energy levels were obtained using an $8 \times 8\,\mathrm{k}\cdot\mathrm{p}$ method as implemented in the 'nextnano^3' program that includes the effects of non-parabolicity, confinement, and strain. The benefits of confinement and strain are in increasing the energy spacing between the heavy and light hole bands, as shown in Fig. 14, and thereby reducing the interband scattering rates. Also beneficial is the strain/confinement-induced decrease in the in-plane mass of the higher lying heavy-hole band. The $Al_{0.8}Ga_{0.2}Sb/In_{0.41}Ga_{0.59}Sb$ valence band offset is 430 meV. The FET discussed in this paper was not intentionally doped. The room-temperature Hall mobility and sheet carrier concentration of the starting material were 1,500 cm^2/V-s and 6.6×10^{11} cm^{-2}, respectively.

Since the InAlSb/InAs barrier/cap layers were identical to that used for the HEMTs in Sect. 2, the fabrication process was the same as that previously described. The drain characteristics obtained for an HFET with a $0.2\,\mu$m gate length are shown in Fig. 15. A threshold voltage of 90 mV was measured at $V_{DS} = -1$ V. Our simulations indicate enhancement-mode should be obtainable with further design improvements. The low-field source-drain resistance at $V_{GS} = -0.4$ V is 8.1 Ω-mm. The cause for this high value is currently under investigation. The dependence of the transconductance on the gate voltage at $V_{DS} = -1.0$ V is shown in Fig. 16. A maximum transconductance of 100 mS/mm is observed at $V_{GS} = -0.1$ V. The gate-source diode I-V characteristic exhibits good rectification and a gate current of 1.5 A/cm^2 at a gate-source bias of 1 V.

The subthreshold slopes at $V_{DS} = -0.05$ V and -1.0 V were 85 mV/dec and 106 mV/dec, respectively. The minimum drain currents observed at $V_{GS} = 0.6$ V for $V_{DS} = -0.05$ V and -1 V were 0.0009 μA/μm and 0.04 μA/μm, respectively. The S-parameters of the HFETs were measured on-wafer from 1 to 40 GHz. Based on the usual 6 dB/octave slope, a maximum f_T of 19 GHz and $f_{\max}$ of 34 GHz were obtained. These values are the highest reported for III-V p-channel HFETs. Further improvements in high-speed, low-voltage performance should be possible with future design and process modifications, including a decrease in gate length, a reduction of the contact and access resistances, and implementation of a T-gate structure.

5. Conclusion

The material growth, fabrication, and characterization of Sb-based HEMTs and p-channel HFETs with an InAlSb upper barrier layer have been presented. The Sb-based HEMTs with a 0.2 μm gate length exhibit an on-resistance of 0.34 Ω-mm for the 0.6 μm source-drain spacing and a transconductance of 1.3 S/mm at only $V_{DS} = 0.2$ V. An intrinsic f_T of 165 GHz is obtained after removal of the gate bonding pad capacitance from an equivalent circuit, corresponding to an $f_T L_g$ product of 33 GHz-μm. The first HEMT MMICs have been demonstrated with excellent performance and high yield. Oxidation stability measurements on un-passivated devices performed over the course of 80 weeks indicate that the InAlSb barrier is very stable in air. InAlSb/InAs HEMTs with an n^+ cap layer have also been demonstrated. As a result, a low on-resistance of 0.35 Ω-mm has been observed for a 1.7 μm source-drain spacing. The 0.28 μm gate length devices exhibited a maximum transconductance at $V_{DS} = 0.2$ V of 1.3 S/mm and an intrinsic $f_T L_g$ product of 26 GHz-μm. Finally, InAlSb/InGaSb p-channel HFETs with a room temperature mobility of 1500 cm^2/V-sec have been demonstrated. At $V_{DS} = -1.0$ V, a maximum transconductance of 100 mS/mm is observed. The 0.2 μm gate length devices exhibit a maximum f_T and $f_{\max}$ of 19 GHz and 34 GHz, respectively. Continued improvements in the material growth, design, and fabrication of these devices will make them attractive candidates in future analog, digital, and mixed-signal applications where high speed and low power consumption will be required.

Acknowledgment

The authors thank Dr. Mark Rosker at the Defense Advanced Research Projects Agency (DARPA) for his support. This work was also supported by the Office of Naval Research.

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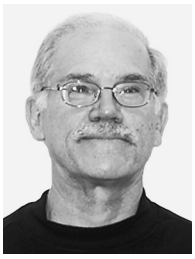
Jeffrey M. Yang (Biography and photo are not available at time of printing)



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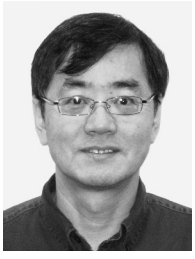

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